L Number	Hits	Search Text	DB	Time stamp
1	171	photosensitive adj polyimide with photoresist	USPAT; US-PGPUB	[illegible] 09:51
2	16	(photosensitive adj polyimide with photoresist) and ashing and @ad<=[illegible]	USPAT; US-PGPUB	[illegible] 10:08
3	31	photosensitive adj polyimide and 438/612,623,688,706,725.ccls.	USPAT; US-PGPUB	[illegible] 10:08
4	93	photosensitive adj polyimide and 430/313,311,317,330.ccls.	USPAT; US-PGPUB	2002/07/31 10:09
5	4	(photosensitive adj polyimide and 430/313,311,317,330.ccls.) and ashing and @ad<=20010105	USPAT; US-PGPUB	2002/07/31 10:09

US-PAT-NO: 6127099

DOCUMENT-IDENTIFIER: US 6127099 A

TITLE: Method of producing a semiconductor device

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A method of producing a semiconductor substrate, particularly one having a buffer coat layer and sealed in a mold resin, is disclosed. The method patterns a polyimide film, etches an insulating film or passivation film using the resulting polyimide pattern as a mask, and then ashes the polyimide pattern by oxygen plasma to thereby obviate the influence of an etchant used for etching. Therefore, the method is capable of reducing the corrosion of portions where a metallic wiring pattern is exposed to the outside. Because the oxygen **ashing** step is followed by heat treatment, the influence of oxygen which would lower the adhesion strength between the polyimide pattern and a mold resin is eliminated. As a result, tight adhesion of the polyimide pattern to the mold resin is insured. Further, when a first heat treatment is effected after the patterning of the polyimide film, a solvent in the polyimide film is evaporated. This reduces degassing in the event of the etching of the passivation film which immediately follows the first heat treatment.

To produce semiconductor device chips, it is necessary that the passivation film and polyimide film be formed with openings in their portions corresponding to scribe lines and bonding pads and be separated therealong. This can be done

if each of the passivation film and polyimide films is patterned through a respective mask implemented by may photoresist. Alternatively, the polyimide film may be patterned first, and then the passivation film may be patterned through the patterned polyimide film. The former method, however, needs a great number of steps which increase manufacturing time. The latter method is disclosed in, e.g., Japanese Patent Laid-Open Publication Nos. 4-015047 and 4-043641. However, the problem with this method, i.e., patterning the passivation film with the hardened polyimide film serving as a mask is that the ions of fluorine-based gas used to etch the passivation film remain on the surface of the polyimide film. The ions cause the exposed portions of Al (aluminum)-based metal to corrode due to moisture in the air. To reduce the corrosion, i.e., to remove the fluorine ions, there has been proposed a method which ashes the surface of the polyimide film by oxygen and then removes only a part of the surface by etching back. This, however, brings about another problem that oxygen for **ashing** dissociates the imide coupling of the polyimide surface and thereby lowers the adhesion of the polyimide to the mold resin.

In accordance with the present invention, a method of producing a semiconductor device comprises the steps of forming a metallic wiring pattern on a semiconductor substrate, forming an insulating film on the metallic wiring pattern, forming a polyimide film on the insulating film, patterning the polyimide film to thereby form a polyimide pattern, selectively etching the insulating film by using the polyimide pattern as a mask, **ashing** the surface of the polyimide pattern by oxygen plasma, and causing the polyimide pattern to

form an imide coupling by heat treatment.

Also, in accordance with the present invention, a method of producing a semiconductor device comprises the steps of forming a metallic wiring pattern on a semiconductor substrate, forming an insulating film on the metallic wiring pattern, forming a polyimide film on the insulating film, patterning the polyimide film to thereby form a polyimide pattern, subjecting the polyimide pattern to first heat treatment, selectively etching the insulating film by using the polyimide pattern as a mask, **ashing** the surface of the polyimide pattern by oxygen plasma, and subjecting the polyimide pattern to second heat treatment.

Subsequently, as shown in FIG. 1B, a 1,000 nm thick passivation film, e.g., silicone nitride (SiN) film 35 is formed on the wiring pattern 34 by CVD (Chemical Vapor Deposition). A **photosensitive polyimide** precursor solution is dropped onto the SiN film by spin coating, thereby forming a polyimide film 36 which is 20,000 nm thick by way of example. As shown in FIG. 1C, the polyimide film 36 is exposed, developed, and then patterned to form, e.g., an opening 37. Then, as shown in FIG. 1D, the film 36 is hardened by heat treatment under optimal conditions, e.g., at a temperature between 300.degree. C. and 400.degree. C. for 60 minutes to 120 minutes. Thereafter, RIE using a fluorine-based gas mixture, e.g., CF.sub.4 --O.sub.2 mixture is effected using the hardened film 36 as a mask, thereby treating the SiN film 35.

CVD to a thickness of 1,000 nm. As shown in FIG. 2D, a **photosensitive polyimide** precursor solution is dropped onto the SiN film 15 by spin. As a

result, the solution is spread over the entire surface of the substrate 11 and forms a polyimide film 16 having a desired thickness, e.g., 2[illegible],000 nm.

As stated above, the embodiment patterns the polyimide film 16, then etches the SiN film 15, and then ashes the substrate 11 by oxygen plasma. Therefore, even when fluorine ions used for etching are left on the surface of the polyimide film 16, they are removed by the oxygen **ashing** together with polyimide. This protects the wiring pattern 14 from corrosion ascribable to fluorine ions. In addition, the heat treatment following the **ashing** allows the imide coupling of the polyimide film 16 dissociated by the **ashing** to be set up again. It follows that the tight contact between the polyimide film 16 and the mold resin is insured and prevents moisture from entering through their interface. The semiconductor device is therefore highly moistureproof.

Referring to FIGS. 3A-3G, a second embodiment of the present invention is shown. First, as shown in FIG. 3A, an insulating film or ground layer 22 is formed on a semiconductor substrate 21 made of Si and formed with devices thereon. A 500 nm high metal film, e.g., Al--Si--Cu film 23 is formed on the insulating film 22 by sputtering or evaporation. As shown in FIG. 3B, photoresist a is applied to the Al--Si--cu film 23 by spin coating, exposed, and then developed to form a resist pattern. Then, RIE using chlorine-based gas is effected with the resist pattern serving as a mask, thereby forming a metallic wiring pattern 24. Subsequently, as shown in FIG. 3C, a passivation film, e.g., SiN film 25 is formed on the wiring pattern 24 by CVD. As shown in FIG. 3D, a **photosensitive polyimide** precursor solution is dropped onto the SiN

film 25 by spin coating. As a result, the solution is spread over the entire surface of the substrate 21 to turn out a polyimide film 26 having a desired thickness, e.g., 20, 00 nm.

This embodiment, like the first embodiment, patterns the polyimide film 26, etches the SiN film 25, and then ashes the surface of the substrate 21 by oxygen **ashing**. This procedure successfully removes fluorine ions together with polyimide and thereby protects the writing pattern 24 from corrosion. Further, the heat treatment following the **ashing** allows the imide coupling of the polyimide film 26 dissociated by the **ashing** to be set up again, so that the film 26 can tightly adhere to the mold resin. In addition, the etching is preceded by the baking for evaporating the solvent of the polyimide film 26. Consequently, degassing during the course of etching is reduced to, in turn, non- stabilize the etching atmosphere and thereby insures the reproducibility of an etcher. In addition, parts built in the etcher are effected little.

For comparison, there were prepared samples produced by the first embodiment, samples produced by the second embodiment, samples produced by a procedure in which etching followed a step of baking a polyimide film (referred to as Prior Art 1), and samples produced by a procedure in which oxygen **ashing** was added t Prior Art 1 after baking (referred to as Prior Art 2). FIG. 4 plots the polyimide-mold adhesion strengths of the above samples. Table 1 shown below lists the results of evaluation of the samples as to peeling at the interface between the polyimide and the mold resin. Table 2 also shown below lists the results of evaluation of the samples as to the corrosion of the portions where

Al is exposed to the outside.

The **photosensitive polyimide** used in the first and second embodiments may be replaced with nonphotosensitive polyimide, if desired. Even with nonphotosensitive polyimide, it is possible to achieve the above advantages only if a polyimide pattern is formed through a mask implemented by a photoresist.

In summary, a method in accordance with the present invention patterns a polyimide film, etches an insulating film or passivation film by using the resulting polyimide pattern as a mask, and then ashes the polyimide pattern by oxygen plasma to thereby obviate the influence of an etchant used for etching. Therefore, the method is capable of reducing the corrosion of portions where a metallic wiring pattern is exposed to the outside. Because the oxygen **ashing** step is followed by heat treatment, the influence of oxygen which would lower the adhesion strength between the polyimide pattern and a mold resin is eliminated. As a result, the tight adhesion of the polyimide pattern to the mold resin is enhanced.

(g) following step (f), oxygen **ashing** a surface of said polyimide pattern by oxygen plasma; and

(h) following step (g), subjecting said polyimide pattern to a second heat treatment of 300.degree. C. to 400.degree. C. to harden said polyimide whereby to reform imide coupling dissociated by the oxygen **ashing** step.

US-PAT-NO: 5982025

DOCUMENT-IDENTIFIER: US 5982025 A

TITLE: Wire fixation structure

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Next, as shown in FIG. 7B, a photoresist mask 206 is formed on the thin metal film 205 by means of photo lithography. The pattern width of this photoresist mask 206 is set to about 50 .mu.m. The **photoresist** mask 206 is formed from a **photosensitive polyimide** film.

As shown in FIG. 7C, the thin metal film 205 is selectively etched with a wet etching method using the photoresist mask 206 as an etching mask, and the printed wires 204 are formed. This wet etching is performed using an etchant such as aqua regia. Then, as shown in FIG. 7D, the photoresist mask 206 is removed by **ashing** or with an organic solvent.

US-PAT-NO: 5807787

DOCUMENT-IDENTIFIER: US 5807787 A

TITLE: Method for reducing surface leakage current on semiconductor intergrated circuits during polyimide passivation

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A method is achieved for reducing the surface leakage current between adjacent bonding pads on integrated circuit substrates after forming a patterned polyimide passivation layer. When the polyimide layer is patterned to open contacts areas over the bonding pads, plasma **ashing** in oxygen is used to remove residual polyimide that otherwise causes high contact resistance, and poor chip yield. This plasma **ashing** also modifies the insulating layer between bonding pads resulting in an unwanted increase in surface leakage currents between bonding pads. The passivation process is improved by using a thermal treatment step in either a nitrogen or air ambient after the plasma **ashing** to essentially eliminate the increased surface leakage current and improve chip yield.

In recent years photosensitive polyimide has attracted considerable interest as the passivation coating over the bonding pads. These photosensitive polyimides have the desirable properties of the more conventional polyimides, such as low dielectric constants, relatively high temperature stability (up to about 450.degree. C.), planarizing properties, etc., but can also be patterned like a photoresist mask, and then remain on the substrate to serve as the

passivation layer. This later attribute is highly desirable for reducing manufacturing cost. Typically a **photosensitive polyimide** precursor is coated on the substrate using, for example, conventional **photoresist** spin coating techniques. The photosensitive polyimide precursor, after a low temperature prebaked, is then exposed through a photo-mask or reticle using, for example, a step and repeat projection aligner and ultra violet (UV) radiation source. The UV exposed portions of the polyimide precursor are crosslinked while leaving unexposed regions over the bonding pads that are not crosslinked. During development, the unexposed polyimide precursor regions over the bonding pads are dissolved away providing openings over the bonding pad areas. Further thermal curing yields a permanent polyimide passivation layer which elsewhere on the substrate. A schematic cross sectional view of a portion of this bonding pad structure having the passivation layers is shown in FIG. 1. Shown are two adjacent bonding pads 4 composed of metal such as aluminum (Al) or an aluminum-copper alloy on a top insulating layer 10 which covers the semiconductor integrated circuit. The contacts between the bonding pads and the integrated circuit are not shown to simplify the drawing. The first passivation layer 12 is deposited over the bonding pads and contact openings 6 are etched in the insulating layer 12 to the bonding pads. The photosensitive polyimide passivation layer 14 is then spin-coated and patterned to provide openings over the bonding pads, as shown in FIG. 1.

Like photoresist processing, when the polyimide is removed over the bonding pads by dissolving away the non-crosslinked polyimide, a polyimide residue remains that can result in unwanted electrical opens or

high contact resistance during testing and/or wire bonding. Typically a mild plasma **ashing** (plasma descumming) step is performed in an oxygen plasma to insure that the trace amounts of the polyimide residue are removed. Unfortunately, this plasma **ashing** can also effect the first passivation layer making the surface conductivity higher, and thereby resulting in significantly higher surface leakage currents across the insulating layer 12 (see FIG. 1) between the bonding pads 4. As semiconductor devices are further reduced in size and the circuit density increased, it will become even more important to minimize leakage currents to maintain circuit performance. Also, with further increase in circuit density and increasing I/O count on the chip the bonding pad pitch will further decrease. Therefore, there is an increasing need in the semiconductor industry to minimize the leakage currents on the integrated circuit.

The method starts by providing a semiconductor substrate on which are already formed the necessary discrete semiconductor devices, such as field effect transistors (FET's), bipolar transistor and similar devices. A multilayer of patterned conducting layers, such as doped polysilicon, silicides and metal with interposed insulating layers, such as chemical vapor deposited silicon oxides, are used to electrically interconnect the device, and thereby form the integrated circuit. The number of metal levels can vary depending on the circuit design, but are typically between about 2 to 4 layers. A top insulating layer, such as a silicon oxide, is provided with contact openings or via holes to the appropriate regions of the integrated circuit to which the

input/out signals and the power and ground plane contacts are to be made. An array of electrically conducting bonding pads are then formed over the contact openings to provide the external wiring contacts for the single or multi-chip carrier. Typically the bonding pads are composed of aluminium or aluminium/copper alloys. Alternatively, aluminum/silicon and aluminum/copper/silicon alloys can also be utilized for making the bonding pads. A first passivation layer, typically a low temperature oxide, such as a plasma enhanced CVD oxide, is deposited over the bonding pads and openings are formed in the first passivation layer to the bonding pads. A much thicker second passivation layer, composed of a photosensitive polyimide, is deposited by spin coating a photosensitive polyimide precursor which is then exposed with ultra violet (UV) radiation through a mask to crosslink the polyimide. The polyimide regions over the bonding pads and over the first passivation layer between the bonding pads is masked from UV exposure (crosslinking) and is dissolved away. Conventional plasma **ashing** in oxygen (O.sub.2) is then performed to remove trace amounts of polyimide residue from the bonding pads for minimizing contact electrical resistance. This **ashing,** unfortunately, increases the surface electrical conductivity on the first passivation layer between the bonding pads and thereby increases the surface leakage currents by about an order of magnitude. By the method of this invention, the substrate is thermally treated in air or nitrogen ambient which reduces the leakage current back to the previous values before the plasma **ashing**. This provides a polyimide passivation layer with improved (lower) surface leakage currents than the conventional process without the thermal treatment.

With continued down scaling of the semiconductor devices dimensions, the device
parametric operating parameters, such as voltage and current, are also reduced,
and therefore, it is very important to minimize the leakage currents in the
circuit. In particular, it is important to maintain a low surface leakage
current on the surface of the first passivation layer 12 between the adjacent
bonding pads 4. However, in conventional processing after forming the bonding
pads, a thick polyimide layer is typically used to passivity the integrated
circuit from contamination and damage. A plasma **ashing** step is then required
to remove residual polyimide over the bonding pad that would otherwise degrade
the electrical contact during testing and wire bonding. Although the plasma
ashing improves the electrical contact it is also known to effect the exposed
passivation layer 12 between the bonding pads 4 results in excessive surface
leakage currents between pads, as depicted in FIG. 1 by the double headed arrow
8.

Referring now more specifically to FIGS. 2 and 3 and referring back to FIG. 1,
the method of this invention is described for eliminating this excess surface
leakage current. The method involves adding a thermal treatment to process for
forming the passivation layer. This heat treatment is performed after the
plasma **ashing** and essentially eliminates the surface leakage current caused by
the plasma **ashing**.

Referring still to FIG. 2, the substrate surface is now passivated a second
time using a second passivation layer 14. This passivation layer is usually
considerably thicker, and besides providing electrical insulation also serves

to protects the substrate from contamination and mechanical damage during subsequent chip processing. The second passivation layer 14 is typically composed of a polyimide, and is preferably a **photosensitive polyimide** which also serves as the **photoresist** mask. One preferred type of photosensitive polyimides is a PIMEL I-8320 AX from a series of polyimides marketed under the trade name PIMEL by the Asahi Chemical Industry Company LTD., of Japan, and can be used for the passivation layer 14. The PIMEL I-8320AX is applied by spin coated using a series of spin speeds ranging between about 1000 to 1500 rpm (revolutions per minute). After a pre-baked at about 95.degree. C. the thickness of the polyimide is between about 9.0 to 12.0 .mu.m (micrometers thick. The photosensitive polyimide precursor (PIMEL I-8320AX) is then exposed using a photomask or reticle in conjunction with a g-line (436 nanometer wavelength) or i-line (365 nm wavelength) stepper. The exposure can be carried out in a g-line and i-line steppers, such as the Nikon, Inc. NSR-1505G2A, Nikon, Inc. NSR-1505i7A steppers, manufactured by Nikon, Inc. of Japan, or PAS-5500/100 stepper manufactured by ASMT, Inc. After developing the polyimide precursor the passivation layer 14 is then cured in nitrogen at a temperature of between about 350.degree. to 400.degree. C. for about 1.0 to 2.0 hours.

After patterning the second passivation layer 14 it is necessary to perform an oxygen plasma **ashing** step to remove residual polyimide that remains on the bonding pads that otherwise results in poor contact resistance and yield loss. This is best understood by reference to TABLE 1 below which shows the contact yield results before and after

The number of test wafers used in the sample size for determining the yields in TABLE 1 was 24. As is seen in TABLE 1, prior to coating the wafer with the polyimide, the bonding pad electrical yield is 92 percent (col. 1), while after coating and patterning the photo-sensitive polyimide, and before plasma **ashing** the yield degrades to 68% (col. 2) due to the polyimide residue on the pads. After the plasma **ashing** in oxygen (O.sub.2) (col. 3) the yield recovers to 91 , which is about equal to the original yield in col. 1. Typically the plasma **ashing** is characterized to remove between about 700 to 750 Angstroms of polyimide.

Although the plasma **ashing** in oxygen reduces the bonding pad contact resistance and improves yield, it also modifies the exposed first passivation layer 12 (see FIG. 1), and thereby increases the surface electrical conductivity between adjacent bonding pads 4. This results in increased surface leakage current between pads, as depicted by the double headed arrow 8 in FIG. 1. For example, the surface leakage current can increase after **ashing** by an order of magnitude., For example the leakage current can increases from about 0.07 to 0.15 nA (nanoampere) to values greater than 1.0 nA, as will be described in more detail in the EXAMPLE provide below.

Now by the method of this invention, the increased surface leakage current resulting from the plasma **ashing** is essentially eliminated by subjecting the substrates to a thermal treatment after the plasma **ashing**. The substrate is preferably heated in an atmospheric ambient (air) to a temperature of between about 250.degree. and 400.degree. C. for a time equal to or greater than 3.0 minutes, and more specifically at a temperature of

250.degree. C. for about 3.0 minutes. For example, the substrate can be heated to 250.degree. C. on a hot plate for about 3.0 minutes. At the higher temperature to further improve the surface leakage currents, the wafers can be annealed in a furnace and then the oxygen can be excluded from the annealing furnace by purging with nitrogen to prevent the oxygen from attaching (damaging) the polyimide at the higher annealing temperatures. For example, a nitrogen purge can be used having less than 40 ppm (part per million) of oxygen, and the treatment temperature can be increased to between about 250.degree. and 400.degree. C., and for a time that is equal or greater than 1.0 hour, and more specifically the substrates can be heated to a temperature of 350.degree. C. for about 2.0 hours to achieve the low leakage current. Either thermal treatment results in about an order of magnitude improvement in the surface leakage current.

As is clearly seen in TABLE 2, after polyimide processing (col. 1) the surface leakage current is between 0.07 to 0.24 nA, and after plasma **ashing** in O.sub.2, increases by about an order of magnitude to between 0.46 to 2.22 nA (col. 2). However, after the thermal treatment in air (col. 3) at 250.degree. C. for 3.0 minutes, by the method of this invention, the surface leakage current is reduced to between 0.05 to 0.14 nA, and after heat treatment in nitrogen (col. 4) at 350.degree. C. for 2.0 hours the surface leakage current is reduced to between 0.01 to 0.14 nA, thereby demonstrating the improvement.

TABLE 1 ____ 2 3 AFTER AFTER 1 POLYIMIDE POLYIMIDE PRIOR TO AND NO AND PRODUCT POLYIMIDE O2 **ASHING** O2 **ASHING**

SAMPLE 92` 68` 91

YIELD

TABLE 2 3 4 1 2
TREAT- TREATMENT TEST
AFTER AFTER MENT IN STURC- POLYTMIDE O2 **ASHING** IN AIR
NITROGEN TURE nanoamp.
nanoamp. nanoamp. nanoamp.
SAMPLE 1
0.24 2.02 0.14 0.04 SAMPLE 2 0.10 0.67 0.05 0.01 SAMPLE
3 1.09 0.64 0.05
0.01 SAMPLE 4 0.11 1.03 0.05 0.01 SAMPLE 5 0.12 1.09
0.09 0.02 SAMPLE 6
0.07 0.46 0.11 0.01 SAMPLE 7 0.15 0.93 0.05 0.05 SAMPLE
8 0.14 0.97 0.09
0.05 SAMPLE 9 0.14 0.75 0.05 0.14

plasma **ashing** in oxygen said substrate surface, and thereby removing polyimide residue on said bonding pads, said plasma **ashing** also causing an increase in the surface leakage current on said first passivation layer between said bonding pads;

11. The method of claim 1, wherein said thermal treatment after said oxygen plasma **ashing** reduces said surface leakage current between said bonding pads by an order of magnitude.

12. The method of claim 1, wherein said thermal treatment after said oxygen plasma **ashing** reduces the surface leakage current from between about 1.0 to 2.0 nanoampere to between about 0.1 to 0.2 nanoampere.

plasma **ashing** in oxygen said substrate surface, and thereby removing polyimide residue on said bonding pads, said plasma **ashing** also causing an increase in the surface leakage current on said first passivation layer between said bonding pads;

22. The method of claim 13 wherein said thermal treatment after said oxygen
plasma **ashing** reduces said surface leakage current between said bonding pads by
an order of magnitude.

23. The method of claim 13 wherein said thermal treatment after said oxygen
plasma **ashing** reduces the surface leakage current from between about 1.0 to 2.0
nanoampere to between about 0.1 to 0.2 nanoampere.

US-PAT-NO: 5310580

DOCUMENT-IDENTIFIER: US 5310580 A

TITLE: Electroless metal adhesion to organic dielectric material with phase separated morphology

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Selective plating through resist masks and activation by forming gases after resist exposure, alkaline treatment or forming gas plasma **ashing** is described in IBM TDB vol. 13, October 1970, p. 1199 and in IBM TDB vol. 25, December 1982, pp. 3336-38.

11. A method of improving adhesion as set forth in claim 10, wherein said **photoresist** layer is **photosensitive polyimide**.